

FW8888 **ALLNET Low Power Utility Server**

Quick Installation Guide





1 System Specification

Processor	Intel Atom N270, 1.6GHz	
Memory Support	2 DDRII 400/533, 2GB Max.	
Storage	CF	
	IDE	
	2 2.5" SATA HDD (option, support RAID0/RAID1)	
Expansion slots	1 PCI slot	
Onboard LAN	1 1000Mbps Fiber Channel LAN	
	5 10/100/1000Mbps LAN	
Front Panel I/O	Power Button	
	Reset Button	
	Power LED	
	Storage Activity LED	
	Dual port USB 2.0 A Type connector	
	DB9 Serial Port Connector	
	1 SFP Fiber Channel Module Connector	_
	5 GbE LAN RJ45 connector	2
Back Panel I/O	2 USB 2.0 A Type Connector	
	VGA Connector	
System FAN	2x 40x40x20mm, 6200rpm system FAN	
Power Supply	250W, 1U Form factor, 100V~240V AC, 50Hz~60Hz, Auto Switch	
Chassis Dimension	426.5(W)x306.0(D)x44.5(H)mm	



2.1 RJ45 (Port1~Port5) LED Indicator Definition:

Link Indicator					
	LED	Color	LED Status	Condition	
	Link Indicator	Orange	On	1000Mbps Link	
		Green	On	100Mbps Link	
			Off	10Mbps Link	
	Activity Indicator	Green	On	Link established	
			Off	No Link	
			Blink	LAN Activity present	

2.2 Fiber Channel (Port 6) Indicator Definition:



LED	Color	LED Status	Condition
Fault	Green	On	Fiber Channel Error
Indicator	Gleen	Off	Fiber Channel Functional
Link	Orango	On	SFP Module Present
Indicator	Urange	Blink	SFP Module not present

2.3 Power and HDD Storage LED Definition

LED	Color	LED Status	Condition
Dowor	Blue	On	System power on
Fower		Off	System power off
Storage	Storage (Storage acting
Activity	Green	Blink	Storage no activity



3 Back Panel



Onboard Connectors, Pin Headers and Jumper Setting:



Item	Description	Item	Description
(4)	DDR2 DIMM1	G	Compact Flash Card Socket
B	DDR2 DIMM2	Θ	32-bit/33MHz PCI slot
6	VAG1,2x8 boxed header	1	USB3, 2x5 pin header, for rear panel USB 2.0
D	PWRCON4PS	J	PWRCON4P
E	40-pin IDE connector	K	CF Master/Slave Setting
F	SATA1 and SATA2	C	Clear CMOS Jumper

- 4.1 System Memory:
 - 4.1.1 Overview:

Intel 945GSE supports DDRII 400/533 memory modules, total 2GB system memory Max.

4.1.2 Configuration:

By Intel 945GSE chipset default, users have to populate DIMM1 to make system work properly. Please refer to the following table for correct memory module population

	DIMM1	DIMM2
1 memory module	V	
2 memory modules	V	V

- 4.1.3 Installing Memory Module:
 - 4.1.3.1 Unlock a DDR2 DIMM socket by pressing the retaining clips outward.
 - 4.1.3.2 Align a DDR2 memory module so that the notch on the module matches the break-on key on the DIMM socket.
 - 4.1.3.3 Firmly insert the memory module into the socket until the retaining clip snap back in place.





Locked Retaining Clip

4.2 IDE connector and Compact Flash card socket :

4.2.1 IDE connector:

IDE connector supports standard ATA 33/66/100 devices.

The pin 20 is removed intentionally for the purpose of dummy-proof.

IDE connector also supports 40 pin IDE DOM (disk on module).

IDE connector is designed to use primary channel and default is set to Slave.

4.2.2. Compact Flash card socket:

Type II CF card connector supports type II CF (compact flash) memory cards.

Please be noted that it is designed as Primary IDE Master, so CF card does not support hot plug feature as normal CF card readers.

4.2.3. CF card Master/Slave Setting:

CF card can be configured as Primary IDE Master / Slave by CF SET J1.



4.3 SATA1 and SATA2:

SATA1 and SATA2 are designed to connect SATA devices via 7-pin SATA cable. Please refer to the following figure for SATA pin definition.



- 4.4 Default Jumper Settings:
 - 4.4.1 Clear CMOS:

Disable: 1-2 pin short (default) Clear CMOS: 2-3 pin short



- 4.5 Other Onboard Connectors:
 - 4.5.1 PWRON4P and PWRCON4PS:

PWRCON4P: provides 12V and 5V DC. PWRCON4P is reserved for supplying 5V and 12V for SATA hard drive or IDE devices.

PWRCON4PS: provides 12V and 5V DC. PWRCON4PS is reserved for supplying 5V and 12V for IDE DOM (Disk On Module)

Please check the following pin-out definition for using PWRCON4P and PWRCON4PS as power source of your device.



4.5.2 VGA1 and USB3 pin 1 : alignment:back panel VGA and USB ports are default connected via cables to main board VGA1 and USB3 respectively.

2

o 10



5 Installation Guide

5.1 Remove the top cover: There are 5 screws fixing the top cover please remove the top cover for the following installation proce.



5.2 Populate DDRII DRAM module: Please refer to section 4.1 when installing DDRII DRAM module.

5.3 Attach storage device.





5.3.2 IDE or SATA devices:

If you take IDE or SATA devices as your storage device, please attach IDE or SATA cable to corresponded connectors on the main board. The PWRCON4P and PWRCON4PS are designed to provide 5V/12V for IDE/SATA devices.

5.4 Close the top cover and secure the top cover with screw.

5.5 Attach AC Power Cord and turn the AC switch on then press PWR BTN to turn on the system.





- 6.1 Boot Sequence:
 - 6.1.1 Default boot sequence: Hard Disk->USB-CDROM-> USB FDD->Boot Other Device

Phoenix – AwardBIOS CMOS Setup Utility Advanced BIOS Features					
CPU Feature IPress Enter	I 🔺 Item Help				
Virus Warning [Disabled]	Menu Level ▶				
CPU LI & LZ Cache [Emabled] CPU L3 Cache [Emabled]	Select Your Boot				
Hyper-Threading Technology[Enabled] Quick Power On Self Test [Enabled]	Device Priority				
First Boot Device [Hard Disk] Second Boot Device [USB-CDROM]					
Third Boot Device [USB-FDD] Boot Other Device [Enabled]					
Boot Up NumLock Status [On] Gate A20 Option [Fast]					
Typematic Rate Setting [Disabled] × Tupematic Rate (Chars/Sec) 6					
× Typematic Delay (Msec) 250 Security Ontion [Setur]					
APIC Mode [Enabled] MPS Version Control For OS[1.4]					
↑↓→+:Move Enter:Select +/-/PU/PD:Value F5:Previous Values	F10:Save ESC:Exit F1:General Help F7: Optimized Defaults				

6.1.2 Changing Hard Disk Boot Priority:

Navigate to "Hard Disk Boot Priority" then press enter

Phoenix - AwardBIOS CMOS Setup Utility Advanced BIOS Features					
▶ CPU Feature ▶ Hard Disk Boot Priority	IPress Enter IPress Enter	1	Item Help		
Virus Warning CPU L1 & L2 Cache	[Disabled] [Enabled]		Menu Level ▶		
CPU L3 Cache Hyper-Threading Technolog	[Enabled] gy[Enabled]		Select Hard Disk Boot Device Priority		
Quick Power On Self Test First Boot Device	[Enabled] [Hard Disk]				
Second Boot Device Third Boot Device	EUSB-CDROMI EUSB-FDD 1				
Boot Uther Device Boot Up NumLock Status	[Enabled] [On]				
Typematic Rate Setting	[Disabled]				
x Typematic Delay (Msec) Security Ontion	250				
APIC Mode MPS Version Control For ([Enabled] DS[1.4]	Ţ			
11++:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help F5:Previous Values F7: Optimized Defaults					

Follow on-screen instruction to change Hard Disk Boot Priority



6.2 Setting Port1 as First LAN in OS:

By Default, Linux initiates PCI Express device driver prior to PCI devices. Therefore, Port1 will not be assigned as eth0 in Linux if you enable Por3~Port6 during Linux install.

Please follow the instruction to disable Port3~6 before installing Linux and get Port1 as eth0.

- 6.2.1 Press "Del" when booting system to enter BIOS CMOS Setup Utility.
- 6.2.2 Navigate to "Advanced Chipset Features" then press enter.

Phoenix - AwardBIUS CMUS Setup Utility			
 Standard CMDS Features Advanced BIDS Features Advanced Chipset Features Integrated Peripherals Power Management Setup PnP/PCI Configurations PC Health Status 	Frequency/Voltage Control Load Optimized Defaults Set Supervisor Password Set User Password Save & Exit Setup Exit Without Saving		
Esc : Quit F9 : Menu in BIOS ↑↓→← : Select Item F10 : Save & Exit Setup			
AT clock, DRAM timings			

6.2.3 Navigate to "Function Ports" then press ener

Phoenix – AwardBIOS CMOS Setup Utility Advanced Chipset Features					
DRAM Timing Selectable	[By SPD]	Item Help			
URS Latency line DRAM RASH to CASH Delay DRAM RASH Precharge Precharge dealy (ERAS) System Memory Frequency SLP_S4H Assertion Width System BIOS Cacheable Video BIOS Cacheable Memory Hole At 15M-16M	LAUGO [Augo] [Augo] [Augo] [Augo] [4 to 5 Sec.] [Enabled] [Disabled] [Disabled]	Menu Level 🕞			
 Function Ports We UGA Setting ** On-Chip Frame Buffer Size DVMT Mode DVMT/FIXED Memory Size Boot Display Panel Scaling Panel Number 	[Press Enter] [8H8] [0047] [12848] [Auto] [Auto] [1]				
†↓→←:Move Enter:Select +/-/ F5:Previous Values	/PU/PD:Value F10:Save I s F7: Optimi	SC:Exit F1:General Help ized Defaults			

6.2.4 Select "Disabled" on LAN Port 3~6.



- 6.2.5 Save and Exit, after system reboots, Port3~6 are disabled during Linux Installation.
- 6.3 Disabling Boot Beep in BIOS:

By default, there is a beep sound when system finishes early stage BIOS boot sequence. To disable the beep during boot sequence, please follow the following procedure:

- 6.3.1 Press "Del" when booting system to enter BIOS CMOS Setup Utility.
- 6.3.2 Navigate to "Advanced Chipset Features" then press enter.

Phoenix - AwardBIOS CMOS Setup Utility				
 Standard CMDS Features Advanced BIDS Features Advanced Chipset Features Integrated Peripherals Fower Management Setup FnP/PCI Configurations FC Health Status 	▶ Frequency/Uoltage Control Load Optimized Defaults Set Supervisor Password Set User Password Save & Exit Setup Exit Without Saving			
Esc : Quit F9 : Menu in BIOS ↑↓→ ← : Select Item F10 : Save & Exit Setup				
AT clock, DRAM timings				

6.3.3 Navigate to "Function Ports" then press enter

Phoenix – AwardBIOS CMOS Setup Utility Advanced Chipset Features					
DRAM Timing Selectable	[By SPD]		I	tem Help	
CAS Latency Time DRAM RASH to CASH Delay DRAM RASH Precharge Precharge dealy (tRAS) System Hemory Frequency SLP_S4H Assertion Width System BIOS Cacheable Video BIOS Cacheable Memory Hole At 15M-16M F function Ports	[Auto] [Auto] [Auto] [Auto] [Auto] [4 to 5 Sec.] [Enabled] [Disabled] [Disabled] [Press Enter]		Menu Le∨	el ⊧	
*** UGA Setting ** On-Chip Frame Buffer Size DUMT Mode DUMTFIXED Memory Size Boot Display Panel Scaling Panel Number	[8MB] [DUMT] [128MB] [Auto] [Auto] [1]				
1↓→←:Move Enter:Select +/-/ F5:Previous Value:	/PU/PD:Value :	F10:Save I F7: Optim:	ESC:Exit ized Defau	F1:General Help lts	

6.3.4 Set "Buzzer" to "Disabled" to disable the boot beep.

LAN Port 3 LAN Port 4 LAN Port 5 LAN Port 6	[Disabled] [Disabled] [Disabled] [Disabled]	Item Help Menu Level ►
PUI-E Compliancy Buzzer	Buzzer	
	Disabled [#] Enabled []	
	14:Move ENTER:Accept ESC:	Abort
	<u>_</u>	
P5 : Previo	us Values P7: 0 hoemix - AwardBlOS CMUS Setu PCI Express Root Port Po	ptimized Defaults p Utility une
F5 : Previou P1	us Values F7: 0 hoenix - AwardBIOS CMUS Setu;	ptimized Defaults p Utility
F5:Previou P1 LAN Port 3 LAN Port 4 LAN Port 5	us Values P7: 0 hoenix - AwardB103 CMUS Setu PCI Express Root Port Po (Disabled) (Disabled) (Disabled)	ptimized Defauits ptihizg unc Item Help Menu Level
P5:Previo P1 LAN Port 3 LAN Port 4 LAN Port 5 LAN Port 5 FCI-E Compliancy P Buzzer	us Ualues P?: 0 locanix - Ausandil 1035 CH15 Setu PCI Express Root Port Pi Clissbied 1 Disabled 1 Disabled 1 Totaabled 1 (Ojsabled 1 (Ojsabled 1 (Ojsabled 1)	ptimized Defaults publity nne Item Help Menu Level
PS:Previo PI LAN Port 3 LAN Port 4 LAN Port 5 ICN Port 6 PCI-E Compliancy M Buzzer	us Ualuces P?: 0 lucentiz - AwardBHOS CHOS Setus PCI Express Root Port Po Disabled J Disabled J Disabled J Disabled J Usabled J Usabled J Usabled J Disabled J	ptimized Defauits ptimized Defauits inc Item Heip Perm Level
PS:Previor PJ LAN Port 3 LAN Port 4 LAN Port 5 TAN Port 5 TAN Port 6 POI-B: Compliancy f Buzzer	us Ualuces P?: 0 locentix - Ausendil1035 CHIS Setu PCI Express Root Port Pi Dissabled 1 Dissabled 1 Dissabled 1 Dissabled 1 Dissabled 1 Dissabled 1 Dissabled 1	ptimized Defaults pHE:lity une Item Help Henn Level P
PS:Previo PJ LAN Port 3 LAN Port 4 LAN Port 5 LAN Port 6 FOI-8 Compliancy N Busser	is Unduce P?: 0 lucentiz - AwardBHOS CHIS Setu PCI Express Root Port Pr (Disabled) (Disabled) (Disabled) (Disabled) tode UQ.(A) (Disabled)	ptimized Defouits ptimity nne Itam Help Perm Level ▶
P5:Previo P1 LAN Port 3 LAN Port 4 LAN Port 5 LAN Port 5 LAN Port 6 P0-E Compliancy P Buzzer	is Unluce P?: 0 localize - Ausredii 1035 CHIS Seta PCI Express Root Port P Disabled J Disabled J Disabled J Disabled J Tote (Disabled J Disabled J	ptimized Defaults ptimized Defaults ptimized tem Help Heno Level

6.3.5 Save and Exit, system will not beep during boot.

6.4 Disabling WOL (Wake on LAN) of Port1:

- By default, Port1 supports WOL (Wake on LAN) feature and is "Enabled". Please follow the following procedure to disable WOL of Port1.
- 6.4.1 Press "Del" when booting system to enter BIOS CMOS Setup Utility.
- 6.4.2 Navigate to "Power Management Setup" and press enter



ACPI Function	[Enabled]	Item Help
ACPI Suspend Type	[S3(STR)]	Manu Yana b
Run VGHDIUS 11 SJ Kesume	INCOJ	nenu Level 🕨
rower nanayement	Infin Saving J	
Uideo Off In Suspend	[Vec]	
Succend Tune	[Ston Grant]	
MODEM Use IRO	[3]	
Suspend Mode	1 Hour	
Soft-Off by PWR-BTTN	[Instant-Off]	
Wake-Up by PCI card	[Enabled]	
Power On by Ring	[Disabled]	
WOL LAN Port 1	[Enabled]	
USB KB Wake-Up From S3	[Disabled]	
Resume by Alarm	[Disabled]	

6.4.4 Select "Disabled" to disable WOL of Port1

Phoenix - Po	wer Management Set	up		
ACPI Function ACPI Suspend Type Run VGABIOS if S3 Resume Power Management	[Enabled] [S3(STR)] [Auto] [Min Saving]	-	Item Menu Level	Help •
Video Uff Method Video Off In Susp WOL LA	N Port 1			
Suspend Type MDDEM Use IRQ Suspend Fode HDD Power Down Soft-Off by PMR-B Wake-Up by PCI ca Power On by Bing WOL LAN Port 1	ed [∎] d []			
Resume by Alarm				
<pre>x Date(of Month) A</pre>	ve ENTER:Accept ES	C:Abort		
		•		
1↓→+:Move Enter:Select +/-	/PU/PD:Value F10:	Save E	SC:Exit F1:0	General Help
tl→+:Move Enter:Select +/- F5:Previous Value Phoenix - Po	/PU/PD:Ualue F10: s F7: AwardBIOS CMOS Se wer Management Set	Save E Optimi tup Uti up	SC:Exit F1:0 zed Defaults lity	General Help
tl++:Move Enter:Select +/- F5:Previous Ualue Phoenix - Po ACPI Function ACPI Suspend Tupe	/PU/PD:Ualue F10: s F7: AwardBIOS CMOS Se wer Management Set [Enabled] [S3(STR)]	Save E Optimiz tup Uti up	SC:Exit F1:0 zed Defaults lity Item	General Help Help
ti++:Hove Enter:Select +/- F5:Previous Value Phoenix - Po ACPI Function ACPI Suspend Type Run GABIOS if S3 Resume Power Management Video Off Method Video Off Method Video Off Method Video Off Method Suspend Type MODEM Use IRQ Suspend Fode Stoff by PWR-BTTN Wake-Up by PCI card Power Do by Ring WoL LaW Port 1 USB KB Wake-Up From S3 Resume by Alarm × Dateof Fonth Alarm	<pre>/PU/PD:Ualue F10: s F10: fmardBIOS CMDS See wer Management Set [Enabled] [S3(STR)] [Auto] [Min Saving] [DPMS] [Yes] [Stop Grant] [3] 1 Hour 15 Min [Instant-Off] [Enabled] [Disabled] [Disabled] [Disabled] [Disabled] [Disabled] [Disabled] [Disabled] [Disabled] [Disabled]</pre>	Save E Optimi: tup Uti up	SC:Exit F1: zed Defaults lity Item Henu Level	Help

6.4.5 Save and Exit to finish the procedure.

6.4.3 Navigate to "WOL LAN Port 1" and press enter.

6.5 Optional SATA RAID

SATA from Intel ICH7M supports Intel RAID 0 and RAID 1 feature. By default, SATA are set to "Enhanced Mode" and "AHCI enabled". Please follow the procedure to change BIOS setting to support Intel IAA RAID.

6.5.1 Press "Del" key during system boot to enter BIOS CMOS Setup Utility.



6.5.2 Navigate to "Integrated Peripherals" and press "Enter"



6.5.3 Navigate to "OnChip IDE Devices" and press "Enter"

Unchip IDE Device	[Press Enter]	Item Help
Super10 Device USB Device Setting	(Press Enter) (Press Enter)	Menn Level 🕨

6.5.4 Navigate to "OnChip IDE Devices" and press "Enter". The following setting are default setting: SATA Mode: AHCI

On-Chip Serial ATA: Enhanced Mode.

IDE HDD Block Mode	[Enabled]	Item Help
IDE DMA transfer access	[Enabled]	
On-Chip Primary PCI IDE	[Enabled]	Menu Level 🕨
IDE Primary Master PIO	[Auto]	
IDE Primary Slave PID	LAutol	[Disabled]: Disabled
IDE Primary Haster UDMA	LAutoJ	SATA Controller.
IDE Primary Slave UDMA	[Auto]	[Auto]: Auto arrange
On-Chip Secondary PCI IDE	LEnabled]	by BIOS.
IDE Secondary Master PIU	LAutoJ	LCombined Model: PATA
IDE Secondary Slave PID [Auto]		and SATA are combined
IDE Secondary Master UDMA	[Auto]	. Max.of 2 IDE drives
IDE Secondary Slave UDMA	LAutoJ	in each channel.
		LEnhanced Model:
		Enable both SATA and
SATA Hode	LAHCIJ	PATA. Max.of 6 IDE
On-Chip Serial ATA	[Enhanced Mode]	drives are supported.
SATA PORT Speed Settings	[Disabled]	ISATA Uniy1: SATA is
PATA IDE Mode	[Secondary]	operating in legacy
		mode.

6.5.5 Navigate to "SATA Mode" and press "Enter" key

Phoen 1× -	AwardBIUS CMUS Setup Ut OnChip IDE Device	111#9
IDE HDD Block Mode	[Enabled]	Item Help
DE DMA transfer access On-Chip Primary Foster PIO DE Primary Naster PIO DE Primary Slave PIO DE Primary Slave UDMA DHC Primary Slave UDMA OHCHIP Secondary Foster PIO DE Secondary Naster PIO DE Secondary Naster UDMA DE Secondary Naster UDMA	(Enabled) (Enabled) (Auto) (Auto) (Auto) (Auto) (Auto) (Auto) (Auto) (Auto) (Auto)	Menu Level ►
www. On_Chin Senial 010 Ser		
SATA Mode	CAHCE J	
On-Chip Serial ATA	[Enhanced Mode]	
SATA PORT Speed Settings	[Disabled]	
PATA IDE Hode	[Secondary]	
SATA Port		
†∔∞:Move Enter:Select •/ P5:Previous Value:	2PU2PD:Ualue F10:Save 1 s F7: Optim	ESC:Exit F1:General Help ized Defaults

6.5.6 Navigate to "RAID" and press "Enter" key

IDE HDD Block Mode	[Enabled]	Item Hely	
IDE DHH transfer a Dh-Chip Primary IDE Primary Master	PCI IDE [Enabled] PCI IDE [Enabled] PIO [Auto]	Menu Level ▶	
IDE Primary Slave; IDE Primary Maste IDE Primary Slave In-Chip Secondary Mas IDE Secondary Sla IDE Secondary Mas IDE Secondary Mas IDE Secondary Sla	SaTA Pode IDE [] NaID [] AHCI []		
SATA Mode SATA Mode Dn-Chip Serial AT SATA PORT Speed S PATA IDE Mode	11:Move ENTER:Accept ES	C:Abort	

6.5.7 SATA1 and SATA2 now are set to support Intel IAA RAID

IDE HDD Block Hode	[Enabled]	Item	Help
DDE DMM transfer access In-Chip Primary PCI IDE DDE Primary Baster PIO DDE Primary Slave UDM DDE Primary Slave UDM IDE Primary Slave UDM IDE Scondary Poster PIO DDE Scondary Slave PIO DDE Scondary Slave UDM DDE Scondary Slave UDM	(Enabled) (Auto) (Auto) (Auto) (Auto) (Auto) (Enabled) (Auto) (Auto) (Auto) (Auto) (Auto)	Menu Level	
sata H ode	[RAID]		
In-Chip Serial ATA	[Enhanced Mode]		
SATA PURT Speed Settings	[Disabled]		
ATA IDE Mode	[Secondary]		

6.5.5 Save and Exit to finish the procedure.

7

LCM Programming Instruction Set

FW8888 has a LCM display that communicates with FW8888 main board via Serial (RS232) interface. In the front panel, there are 4 buttons (up, down, enter and escape) that can control the uP of LCM module to display or configured customer desired information of FW8888.

7.1 Connector (COM2) Pin-Out Definition



7.2 Serial Interface Protocol:

Universal Asynchronous Receiver Transmitter Baud Rate: 9600 bps Data: 8 bit Parity Check: No Stop Bit: 1

- 7.3 LCM Initial Setting
 - 7.3.1 16 character, 2 lines. Character format is: 5x7+cursor
 - 7.3.2 Cursor display means shift right 1 character
 - 7.3.3 When character reads in to LCM display, position address adds 1bit and cursor shifts to right 1 character automatically.

7.4 Instruction Set:

Clear Display

Direction	Host to LCM
Command	0x10, 0x01
Explain	Clears all currently displayed characters
Response	LCM to Host
Command	0x11(Acknowledge OK)
	0x14(Acknowledge Fail and no action executed)

Return Home

Direction	Host to LCM
Command	0x10, 0x02
Explain	Returns cursor display to character 1 of line 1
Response	LCM to Host
Command	0x11(Acknowledge OK)
	0x14(Acknowledge Fail and no action executed)

Display On/Off

Direction	Host to LCM
Command	0x10, 0x08(entire display off)
	0x10, 0x0C(entire display on & cursor off)
	0x10, 0x0E(entire display & cursor on)
Explain	Setting LCM to show cursor or not
	Setting LCM display area all On or all Off
Response	LCM to Host
Command	0x11(Acknowledge OK)
	0x14(Acknowledge Fail and no action executed)



Turn On/Off Backlight

Direction	Host to LCM
Command	0x10, 0x38 (turn off backlight)
	0x10, 0x39 (turn on backlight)
Explain	Turn on or turn off backlight
Response	LCM to Host
Command	0x11(Acknowledge OK)
	0x14(Acknowledge Fail and no action executed)

SeDisplay Character Position Address

Direction	Host to LCM					
Command	0x10, 0x80~0x8F (Line 1, character 1~16)					
	0x10, 0xC0~0xCF (Line 2, character 1~16)					
Explain	Set character display position					
Response	LCM to Host					
Command	0x11(Acknowledge OK)					
	0x14(Acknowledge Fail and no action executed)					

Write Display Data into Position Address

Direction	Host to LCM					
Command	0x12, 0x00~0xFF (ASCII code and extension ROM code)					
Explain	Display character on the position address.					
	Position address will automatically add 1 bit after data written in					
	Position address available: 0x80~0x8F, 0xC0~0xCF					
Response	LCM to Host					
Command	0x11(Acknowledge OK)					
	0x14(Acknowledge Fail and no action executed)					

Button Return Values



Direction	LCM to Host
Command	0x15, Up
	0x16, Down
	0x17, Enter
	0x18, Escape
Explain	LCM will return the corresponded value to Host when key pressed

Appendix:

A. ASCII Code

Char	Hex	Char	Hex	Char	Hex	Char	Hex
(nul)	0x00	(sp)	0x20	@	0x40	`	0x60
(soh)	0x01	!	0x21	А	0x41	а	0x61
(stx)	0x02	"	0x22	В	0x42	b	0x62
(etx)	0x03	#	0x23	С	0x43	с	0x63
(eot)	0x04	\$	0x24	D	0x44	d	0x64
(enq)	0x05	%	0x25	Е	0x45	е	0x65
(ack)	0x06	&	0x26	F	0x46	f	0x66
(bel)	0x07	'	0x27	G	0x47	g	0x67
(bs)	0x08	(0x28	Н	0x48	h	0x68
(ht)	0x09)	0x29	I	0x49	i	0x69
(nl)	0x0a	*	0x2a	J	0x4a	j	0x6a
(vt)	0x0b	+	0x2b	К	0x4b	k	0x6b
(np)	0x0c	,	0x2c	L	0x4c	I	0x6c
(cr)	0x0d	-	0x2d	М	0x4d	m	0x6d
(so)	0x0e	-	0x2e	N	0x4e	n	0x6e
(si)	0x0f	/	0x2f	0	0x4f	0	0x6f
(dle)	0x10	0	0x30	Р	0x50	р	0x70
(dc1)	0x11	1	0x31	Q	0x51	q	0x71
(dc2)	0x12	2	0x32	R	0x52	r	0x72
(dc3)	0x13	3	0x33	S	0x53	S	0x73
(dc4)	0x14	4	0x34	Т	0x54	t	0x74
(nak)	0x15	5	0x35	U	0x55	u	0x75
(syn)	0x16	6	0x36	V	0x56	v	0x76
(etb)	0x17	7	0x37	W	0x57	w	0x77
(can)	0x18	8	0x38	Х	0x58	х	0x78
(em)	0x19	9	0x39	Y	0x59	У	0x79
(sub)	0x1a	:	0x3a	Z	0x5a	z	0x7a
(esc)	0x1b	;	0x3b	[0x5b	{	0x7b
(fs)	0x1c	<	0x3c	١	0x5c		0x7c
(gs)	0x1d	=	0x3d]	0x5d	}	0x7d
(rs)	0x1e	>	0x3e	^	0x5e	~	0x7e
(us)	0x1f	?	0x3f	_	0x5f	(del)	0x7f

24.

Weitere Einstellungen und Managementfunktionen entnehmen Sie bitte dem Handbuch auf der beiliegenden CD. Für weitere Informationen oder Online-Ressourcen besuchen Sie bitte unsere Website: http://www.allnet.de

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